response thereto. Claims 1, 17, 29 and 34-36 have been amended to more particularly point out and distinctly claim the present invention. No new matter has been added. Claims 1-40 are respectfully submitted for consideration.

The drawings were objected to by the Office because it was alleged that not every feature of the claims is illustrated in the drawings. More specifically, it was alleged that "at least three macro circuits each including a logic circuit and a memory circuit" is not illustrated. Applicant has amended independent claims 1, 17, 29 and 34-36 to indicate that each of the macro circuits includes either a logic circuit or a memory circuit. As such, Applicant respectfully asserts that the drawings now illustrate every feature of the claims and Applicant requests withdrawal of the objection thereto.

Claims 1-3, 6-11, 15-18, 21-24, 27-30 and 33-40 were rejected under 35 U.S.C. §102(e) as being anticipated by *Sato et al.* (U.S. Patent No. 5,930,187). Claims 4, 5, 12-14, 19, 20, 25, 26, 31 and 32 were objected to as being dependent on rejected claims but were also indicated as containing allowable subject matter. Applicant respectfully submits that each of claims 1-40, as submitted herein, recites subject matter which is neither disclosed nor suggested in the cited prior art.

In the present invention, at least three macro circuits are connected into a loop (half loop), and signal transmission or signal reception are selectively carried out in accordance with the destination of the signal. Specifically, in claims 1 or 34, at least three macro circuits are connected to one another into a loop to transmit signals in a single specified direction through signal lines in synchronization with a clock signal, and each of the macro circuits receives signals at input terminals thereof, accepts the received signals if the received signals are destined therefore, and transfers the

received signals to output terminals thereof without accepting the received signals if the received signals are not destined therefore.

Further, in claims 17 or 35, a first and second to "n"th macro circuits (n being an integer larger than 3) are connected to one another into a half loop with output terminals of the first macro circuit being at the start of the half loop and input terminals of the first macro circuit at the end of the half loop, to transmit signals in a single specified direction through signal lines in synchronization with a clock signal; the first macro circuit accepts signals received by the input terminals thereof if the received signals are destined for the first macro circuit, and each of the second to "n"th macro circuits accepts signals received by input terminals thereof if the received signals are destined therefore and transits the received signals as they are from output terminals thereof, without accepting the received signals, if the received signals are not destined therefore.

In addition, in claims 29 or 36, first to "m-1"th macro circuits (m being an integer larger than 2) are connected to one another into a half loop with external input terminals being at the start of the half loop and input terminals of the "m"th macro circuit at the end of the half loop, to transmit test signals in a single specified direction through signal lines in synchronization with a clock signal, each of the first to "m-1"th macro circuits accepts the test signals received by the input terminals thereof if the test signals are destined therefore and transmits the test signals from the output terminal thereof if the test signals from the output terminals thereof if the test signals are not destined therefore, and the "m"th macro circuit accepts the test signals received by the input terminals thereof if the test signals are destined therefore.

Sato et al. (U.S. Patent No. 5,930,187) discloses one-chip LSI having logic section 1, a data input/output section 2, a memory macro section 3, and a test control section 4. It is noted that a plurality of memory blocks or a plurality of memory cells in the memory macro section 3 are not connected in a loop or a half loop. The independent claims all recite that the macro circuits are connected by a loop or a half loop, and therefore, Applicant respectfully asserts that the anticipation rejection is improper for failing to teach all of the elements of the claims.

In the present invention, as recited in claims 1, 17, 29 and 34-36, a plurality of macro circuits (at least three) are connected into a loop or a half loop by signal lines without using a common bus, and thereby signal transmission efficiency is improved and signal transmission management is simplified. Specifically, *Sato et al.*, where the common bus is used, an electronic circuit system for managing the use of the common bus becomes deteriorated. Therefore, *Sato. et al.* does not teach or suggest the above special characteristics of the invention.

As such, Applicant respectfully asserts that the rejection of claims 1-3, 6-11, 15-18, 21-24, 27-30 and 33-40 is improper for failing to teach or suggest all of the elements of the claims. Applicant therefore respectfully requests that claims 1-40 be found allowable, and this application be passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 1-2300.

Respectfully submitted,

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MARKED-UP COPY OF CLAIMS

1. (Amended) An electronic circuit system comprising:

at least three macro circuits each including a logic circuit [and] or a memory circuit, and having a plurality of input terminals and a plurality of output terminals; and

a plurality of signal lines for connecting the macro circuits to one another into a loop to transmit signals in a single specified direction through the [loop] signal lines in synchronization with a clock signal,

each of the macro circuits receiving the signals at the input terminals thereof, accepting the received signals if the received signals are destined thereto, and transferring the received signals to the output terminals thereof without accepting the received signals if the received signals are not destined thereto.

17. (Amended) An electronic circuit system comprising:

a first macro circuit constituted by a logic circuit having a plurality of input terminals and a plurality of output terminals;

second to "n"th macro circuits (n being an integer larger than 3) each including a memory circuit but no logic circuit, and having a plurality of input terminals and a plurality of output terminals; and

a plurality of signal lines for connecting the first to "n"th macro circuits to one another into a half loop with the output terminals of the first macro circuit being at the start of the half loop and the input terminals of the first macro circuit at the end of the half loop, to transmit signals in a single specified direction through the [half loop] signal lines in synchronization with a clock signal,

the first macro circuit accepting signals received by the input terminals thereof if the received signals are destined for the first macro circuit,

each of the second to "n"th macro circuits accepting signals received by the input terminals thereof if the received signals are destined thereto and transmitting the received signals as they are from the output terminals thereof, without accepting the received signals, if the received signals are not destined thereto.

29. (Amended) An electronic circuit system comprising:

a plurality of external input terminals for receiving test signals;

first to "m-1"th macro circuits (m being an integer larger than 2) each having a plurality of input terminals and a plurality of output terminals for receiving and transmitting the test signals;

an "m"th macro circuit having input terminals for receiving the test signals; and

a plurality of signal lines for transmitting the test signals and connecting the external input terminals and the first to "m"th macro circuits to one another into a half loop with the external input terminals being at the start of the half loop and the input terminals of the "m"th macro circuit at the end of the half loop, to transmit the test signals in single specified direction through the [half loop] signal lines in synchronization with a clock signal,

each of the first to "m-1"th macro circuits accepting the test signals received by the input terminals thereof if the test signals are destined thereto.

the "m"th macro circuit accepting the test signals received by the input terminals thereof if the test signals are destined thereto.

34. (Amended) A signal transmission method comprising the steps of:

connecting at least three macro circuits each having a plurality of input terminals and a plurality of output terminals to one another [through signal lines] into a loop to transmit signals in a single specified direction through signal lines in synchronization with a clock signal; and

making each of the macro circuit accept signals received by the input terminals thereof if the received signals are destined thereto and transfer the received signals as they are, without accepting them, to the output terminals thereof if the received signals are not destined thereto.

35. (Amended) A signal transmission method comprising the steps of:

connecting first to "n"th macro circuits (n being an integer larger than 3) each having a plurality of input terminals and a plurality of output terminals to one another through signal lines into a half loop, the first macro circuit being a logic circuit, each of the second to "n"th macro circuits including a memory circuit but no logic circuit and having a plurality of input terminals and a plurality of output terminals, the output terminals of the first macro circuit being at the start of the half loop, the input terminals of the first macro circuit being at the end of the half loop to transmit signals in a single specified direction through the [half loop] signal lines in synchronization with a clock signal;

making each of the second to "n"th macro circuits accept signals received by the input terminals thereof if the received signals are destined thereto and transmit the received signals are destined thereto and transmit the received signals from the output

terminals thereof, without accepting the received signals, if the received signals are not destined thereto; and

making the first macro circuit accept signals received by the input terminals thereof if the received signals are destined thereto.

36. (Amended) A signal transmission method comprising the steps of:

connecting a plurality of external input terminals for receiving test signals, first to "m-1"th macro circuits (m being an integer greater than 2) each having a plurality of input terminals and a plurality of input terminals for receiving and transmitting the test signals, and an "m"th macro circuit having a plurality of input terminals for receiving the test signals, to one another into a half loop through signals lines for transmitting the test signals, the external input terminals being at the start of the half loop, the input terminals of the "m"th macro circuit being at the end of the half loop to transmit the test signals in a single specified direction through the [half loop] signal lines in synchronization with a clock signal;

making each of the first to "m"th macro circuits accept the test signals received by the input terminals thereof if the test signals are destined thereof and transmitting the test signals from the output terminals thereof, without accepting the test signals, if the test signals are destined thereto; and

making the "m"th macro circuit accept the test signals received by the input terminals thereof if the test signals are destined thereto.